

DQ80251

Revolutionary Quad-Pipelined Ultra High Performance 16/32-bit Microcontroller v. 6.05

OVERVIEW

DQ80251 is a revolutionary **Quad-Pipelined ultra-high performance, speed optimized** soft core, of a 16-bit/32-bit embedded microcontroller. The core has been designed with a special concern for performance to power consumption ratio. This ratio is extended by an **advanced power management PMU unit**. This product is built based on 11 years of DCD's know-how, with triumphant 8051 architectures. DQ80251 soft core is 100% binary-compatible with the industry standard 16-bit 80C251 and 8-bit 80C51 microcontrollers. There are two working modes of the DQ80251: BINARY (where original 80C51 compiled code is executed) and SOURCE (native 80C251 mode, using all DQ80251 performance). DQ80251 has built-in, configurable DoCD-JTAG on chip debugger, supporting Keil DK251 and standalone DoCD debug software. **Dhrystone 2.1 benchmark program runs 56.8 times faster than the original 80C51 and 4.81 times faster, than the original 80C251 at the same frequency.** This performance can be also exploited to great advantage in **low power** applications, where the core can be clocked over fifty times slower, than the original implementation, for no performance penalty. Additionally, compiled code size for SOURCE mode is about **2 times smaller**, comparing to identical standard 8051 code, since DQ80251 instructions are more effective.

The DQ80251 is delivered with **fully automated testbench** and **complete set of tests**, allowing easy package validation, at each stage of SoC design flow.

CPU FEATURES

- 100% binary compatible with industry standard 80C251 implementing BINARY and SOURCE modes
- Single clock period per most of instructions
- **Quad-Pipelined** architecture enables to execute **56.8** times faster than the original 80C51 and **4.81** times faster than 80C251 at the same frequency
- **Up to 53.411 VAX MIPS at 100 MHz**
- Up to 8M bytes of Program Memory
- Up to 32k bytes of internal (on-chip) Data Memory
- Up to 8M bytes of external (off-chip) Data Memory
- Up to 16 MB of total memory space for CODE and DATA
- 32k bytes of extended stack space
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable Extended Data Memory Wait States solution for wide range of memories speed

- De-multiplexed Address/Data bus to allow easy connection to memory
- Full Program Memory writes
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready

PERFORMANCE

The following table gives a survey about the Core area and performance in ASICs Devices:

Technology	Speed grade	Area Min [gates]	Area Full [gates]	F _{max}
0.18u	typical	15 100	28 600	120 MHz
0.13u	typical	15 000	28 000	200 MHz
0.09u	typical	14 500	26 100	300 MHz

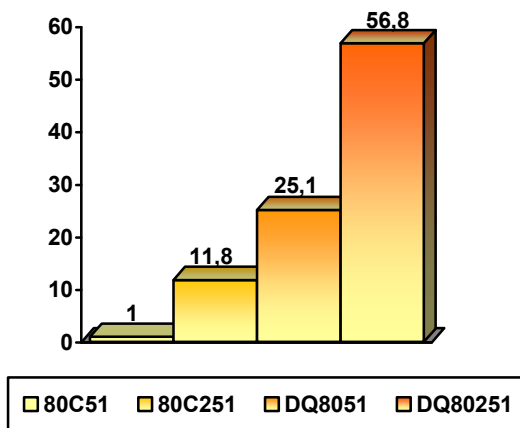
Core performance in ASIC devices – **results given for working system with connected CODE and DATA memories**. DoCD debugger increases core size about 3000 gates.

Dhrystone Benchmark Version 2.1 was used to measure Core performance. The following table gives a survey about the DQ80251 performance, in terms of VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
80C251	0,11102	11,79
DQ8051	0,22369	23,77
DQ80251	0,53411	56,76

Core performance in terms of DMIPS per MHz

VAX MIPS ratio



PERIPHERALS

- DoCD™ debug unit
 - Processor execution control
 - Run, Halt
 - Step into instruction
 - Skip instruction
 - Read-write all processor contents
 - Program Counter (PC)
 - Program Memory
 - Internal (direct) Data Memory
 - Special Function Registers (SFRs)
 - Extended Data Memory
 - Code execution breakpoints
 - two real-time PC breakpoint
 - unlimited number of real-time OPCODE breakpoints
 - Hardware execution watch-points at
 - Internal Data Memory
 - Extended Data Memory
 - Special Function Registers (SFRs)
 - Hardware watch-points activated at a certain
 - address by any write into memory
 - address by any read from memory
 - address by write into memory a required data
 - address by read from memory a required data
 - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
 - JTAG Communication interface
- Power Management Unit
 - Power management mode
 - Switchback feature
 - Stop mode
- Interrupt Controller
 - 4 priority levels
 - 2 external interrupt sources
 - 3 interrupt sources from peripherals
- Four 8-bit I/O Ports
 - Bit addressable data direction for each line
 - Read/write of single line and 8-bit group
- Two 16-bit timer/counters
 - Timers clocked by internal source
 - Auto reload 8-bit timers
 - Externally gated event counters

- Full-duplex serial port
 - Synchronous mode, fixed baud rate
 - 8-bit asynchronous mode, fixed baud rate
 - 9-bit asynchronous mode, fixed baud rate
 - 9-bit asynchronous mode, variable baud rate

CONFIGURATION

The following parameters of the DQ80251 core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Program Memory size - 64kB - 8MB
- Internal Data Memory size - 1kB - 32kB
- Extended Data Memory size - 1kB - 8MB
- Program Memory Interface - synchronous
- asynchronous
- Data Memory Interface - synchronous
- asynchronous
- Interrupts - subroutines
- location
- Power Management Mode - used
- unused
- Stop mode - used
- unused
- DoCD™ debug unit - used
- unused

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

DELIVERABLES

- ◆ Source code:
 - VERILOG Source Code or/and
 - VHDL Source Code or/and
 - FPGA Netlist
- ◆ VERILOG or VHDL test bench environment
 - NCSim automatic simulation macros

- ModelSim automatic simulation macros
- Active-HDL automatic simulation macros
- Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

DESIGN FEATURES

- ◆ **PROGRAM MEMORY:**
The DQ80251 soft core is dedicated for operation with Internal and External Program Memory up to 8MB of size. It can be configured as synchronous or asynchronous.

◆ **DATA MEMORY:**

The DQ80251 can address synchronous Internal Data Memory of up to 32k bytes and up to 8MB of External Data Memory. The External Data Memory interface can be configured as synchronous or asynchronous. XDATA memory (from 8051/ 80390) is inside the EDATA space.

◆ **USER SPECIAL FUNCTION REGISTERS:**

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DQ80251 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF, in the same manner as core SFRs and may occupy any address, that is not occupied by a core SFR.

◆ **WAIT STATES SUPPORT:**

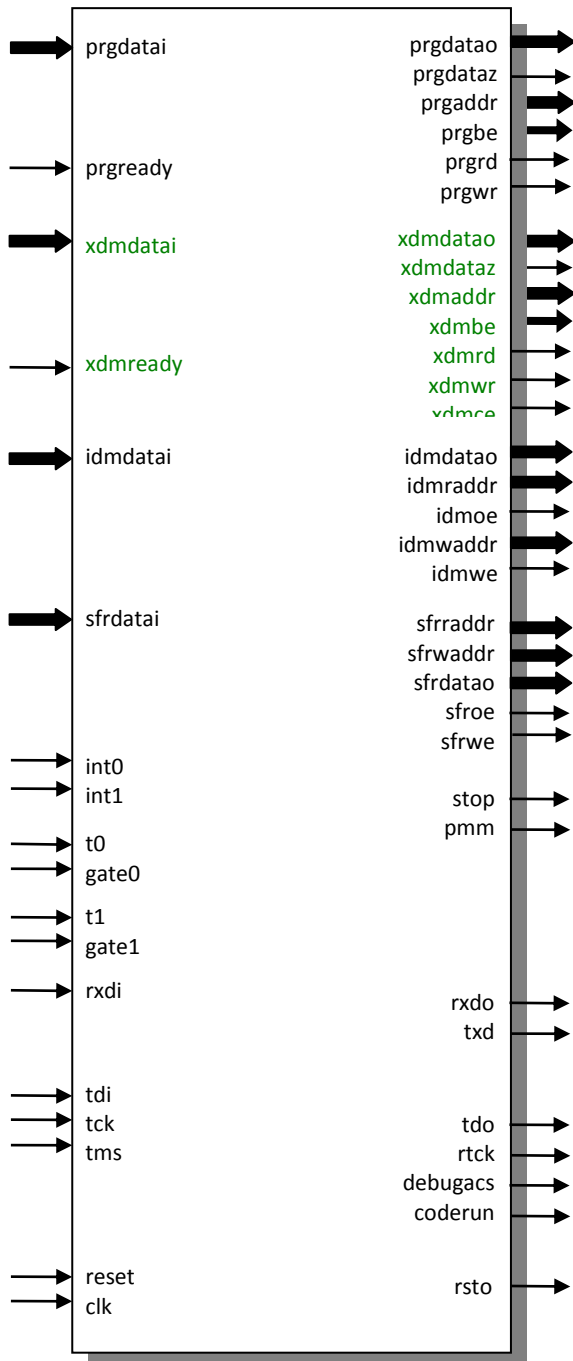
The DQ80251 soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and Extended Data memory may assert a memory WAIT signals, to hold up CPU activity for required period of time.

PINS DESCRIPTION

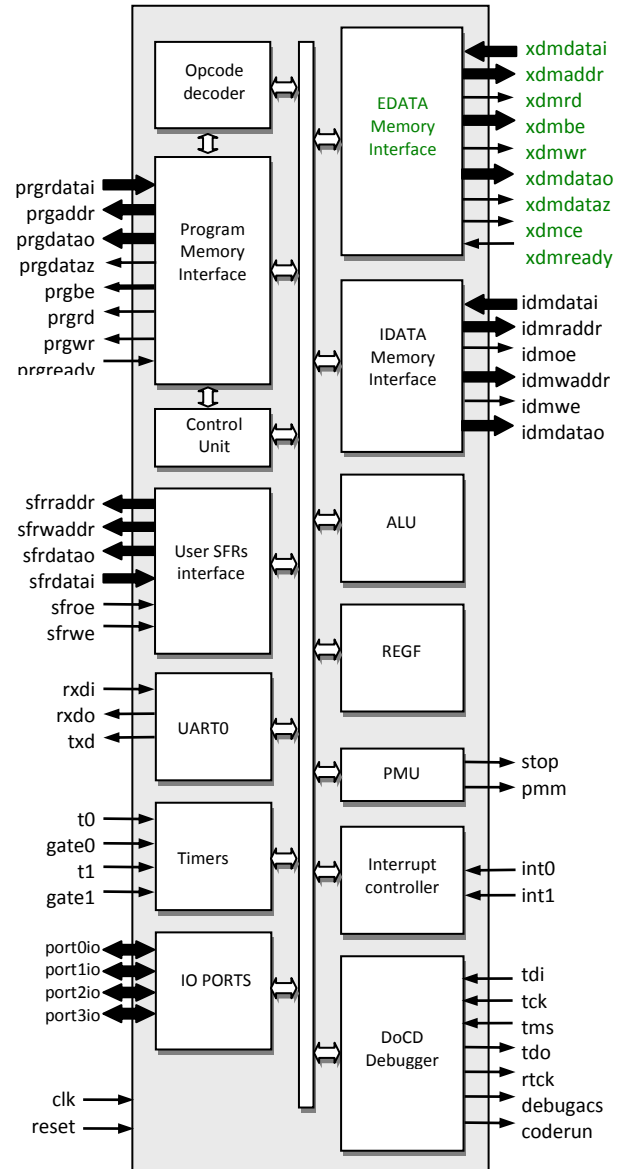
PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset input
port0i	input	Port 0 input
port1i	input	Port 1 input
port2i	input	Port 2 input
port3i	input	Port 3 input
prgdatai	input	Data bus from CODE Memory
xdmdatai	input	Data bus from EDATA Memory
xdmready	input	EDATA memory data ready
prgready	input	CODE memory data ready
idmdatai	input	Data bus from IDATA memory
sfrdatai	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
t0	input	Timer 0 input
t1	input	Timer 1 input

PIN	TYPE	DESCRIPTION
gate0	input	Timer 0 gate input
gate1	input	Timer 1 gate input
rxdi0	input	Serial receiver input 0
tdi	input	DoCD™ TAP data input
tck	input	DoCD™ TAP clock input
tms	input	DoCD™ TAP mode select input
rsto	output	Reset output
port0o	output	Port 0 output
port1o	output	Port 1 output
port2o	output	Port 2 output
port3o	output	Port 3 output
prgaddr	output	CODE memory address bus
prgdatao	output	Data bus for CODE memory
prgdataz	output	Turn CODE bus into 'Z' state
prgbe	output	CODE data bus byte enable
prgrd	output	CODE memory read
prgwr	output	CODE memory write
xmaddr	output	Address bus for EDATA memory
xmdatao	output	Data bus for EDATA memories
xmdataz	output	Turn EDATA bus into 'Z' state
xdmbe	output	EDATA data bus byte enable
xdmrd	output	Extended data memory read
xdmwr	output	Extended data memory write
xdmce	output	Extended data memory chip enable
idmaddr	output	IDATA Memory address bus
idmdatao	output	Data bus for IDATA memory
idmoe	output	Internal data memory output enable
idmwe	output	Internal data memory write enable
sfraddr	output	Read address bus for user SFR's
sfrwaddr	output	Write address bus for user SFR's
sfrdatao	output	Data bus for user SFR's
sfroe	output	User SFR's read enable
sfrwe	output	User SFR's write enable
tdo	output	DoCD™ TAP data output
rtck	output	DoCD™ return clock line
debugacs	output	DoCD™ accessing data
coderrun	output	CPU is executing an instruction
pmm	output	Power management mode indicator
stop	output	Stop mode indicator
rxdo0	output	Serial receiver output 0
txd0	output	Serial transmitter output 0

SYMBOL



BLOCK DIAGRAM



UNITS SUMMARY

ALU – 16/32-bit Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW, PSW1), (B) registers and related logic, such as arithmetic unit, logic unit, multiplier and divider.

REGFILE – Contains complete set of 80251 dedicated: 8-bit {R0, R1, ..., R15} registers, 16-bit {WR0, WR2, ..., WR30} and 32-bit {DR0, DR4, ..., DR28, DR56, DR60} registers.

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages the execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory (CODE) can be also written. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States and allows core to work with different speed program memories. It works with synchronous or asynchronous memories.

EDATA Memory Interface - Contains memory access related registers. It performs the Extended Data Memory (EDATA) addressing and data transfers. EDATA read/write cycle length can be programmed by user. EDATA covers also XDATA space from 80C51. This feature is called EDATA Memory Wait States and allows core to work with different speed memories. It is fully configurable. It works with synchronous or asynchronous memories.

Internal Data Memory Interface – Internal Data Memory interface controls access into the whole 32kB of IDATA memory. It contains 16-bit Stack Pointer (SP) register and related logic. It is fully configurable from 1 kB to 32 kB.

SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. All SFR registers are bit addressable. User defined external devices, can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

Interrupt Controller – Four Levels interrupt control module is responsible for the interrupt manage system, for external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IPH, IPL) and (TCON) registers. Its upgraded version can be extended by extra user's dedicated interrupt

sources. Interrupt vectors locations and spacing are fully configurable.

Timers – System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of the second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2 (if present in system).

Ports - Block contains 8051 general purpose I/O ports. Each of ports pin can be read/write as a single bit or as a 8-bit bus P0, P1, P2, P3

Power Management Unit – contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It's highly desirable, when microcontroller is planned to be used in portable and power critical applications.

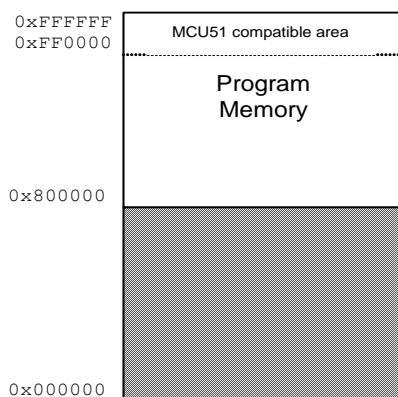
DoCD™ Debug Unit – a real-time hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write



any contents of microcontroller, including all registers, internal and external data, program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, REGFILE and also on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins - CODERUN and DEBUGACS, indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by **DoCD™** debugger. The **DoCD™** system includes JTAG interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

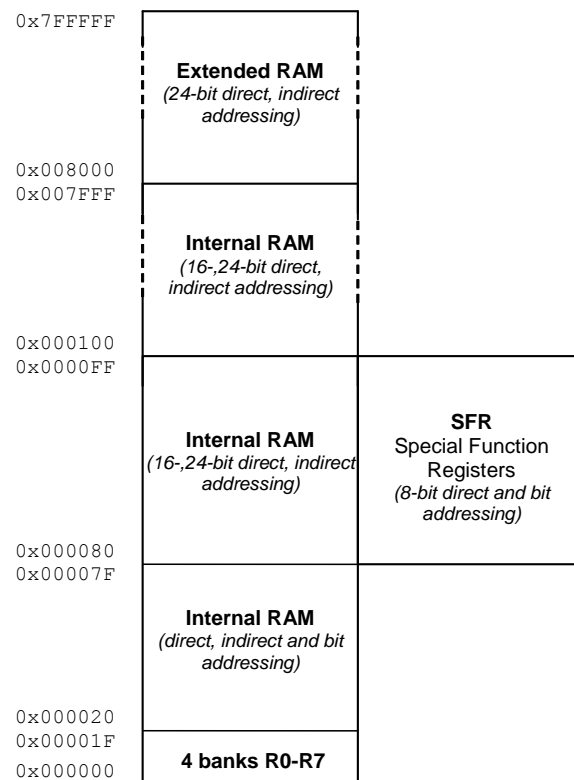
PROGRAM CODE SPACE

The program memory space begins at address 0x800000 and ends at 0xFFFFF address. It gives 8MB of code memory. The 64kB memory area, ranged 0xFF0000 to 0xFFFFF, is intended for MCU51 compatible code. After each reset, the CPU starts execution in the program memory, at location 0xFF0000. Each interrupt has its own start address for its service routine. The interrupt vectors are also mapped, starting at 0xFF0000 location.



DATA MEMORY

The DQ80251 has up to 32k bytes of internal data memory (IDATA) and up to 8MB of extended data memory (EDATA).



The lower internal RAM consists of four register banks, with eight registers each. The current bank is selected by PSW register. A bit addressable segment is mapped in range 0x20 to 0xFF and covers part of internal RAM and all SFR area. With the **16-, 24-bit direct or indirect** addressing mode, 0x80 to 0xFF range of the internal memory is addressed. With the **8-bit direct** addressing mode, range 0x80 to 0xFF the SFR memory area, is accessed. Extended RAM space begins just after end of Internal RAM memory chip. For example, if Internal RAM has 1kB size, then Extended RAM starts at 1 kB address.

CONTACT

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